**实验报告**

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| 专业 | 软件工程 | | 课程名称 | 计算机组成原理课程设计 | |
| 任课老师 | 仇建 | 指导老师 | 仇建 | 机位号 |  |
| 实验序号 | 2 | 实验名称 | 超前进位加法器设计实验 | | |
| 实验时间 |  | 实验地点 |  | 实验设备号 |  |
| **一、实验程序源代码** | | | | | |
| 程序源代码  module module(A,B,C0,F,C4);  input [3:0] A,B;  input C0;  output [3:0] F;  output C4;  wire [3:0] A;  wire [3:0] B;  wire C0;  wire [3:0] F;  wire C4;  //A 异或 B 异或 C  assign F[0] = A[0]^~B[0]^~C0;  //A,B,C1 任意两者为 1  assign C1 = (A[0]&B[0])|((A[0]|B[0])&C0);  //前一位输出Ci+1作为后一位输入Ci  assign F[1] = A[1]^~B[1]^~C1;  assign C2 = (A[1]&B[1])|((A[1]|B[1])&C1);  assign F[2] = A[2]^~B[2]^~C2;  assign C3 = (A[2]&B[2])|((A[2]|B[2])&C2);  assign F[3] = A[3]^~B[3]^~C3;  assign C4 = (A[3]&B[3])|((A[3]|B[3])&C3);  endmodule  仿真代码  module Test;  // Inputs  reg [3:0] A;  reg [3:0] B;  reg C0;  // Outputs  wire [3:0] F;  wire C4;  // Instantiate the Unit Under Test (UUT)  Module2 uut (  .A(A),  .B(B),  .C0(C0),  .F(F),  .C4(C4)  );  initial begin  // Initialize Inputs  A = 0;  B = 0;  C0 = 0;  // Wait 100 ns for global reset to finish  #100;    // Add stimulus here  A=4'b1100;B=4'b1011;C0=1'b0;  #100;  A=4'b1011;B=4'b0010;C0=1'b1;  #100;  A=4'b1011;B=4'b1101;C0=1'b0;  #100;  A=4'b1010;B=4'b0010;C0=1'b1;  #100;  A=4'b0111;B=4'b1000;C0=1'b0;  #100;  A=4'b0011;B=4'b0100;C0=1'b1;  #100;  A=4'b1001;B=4'b0001;C0=1'b0;  end    endmodule | | | | | |
| **二、仿真波形** | | | | | |
| ISim (O.87xd) - [Default.wcfg] | | | | | |
| **三、电路图** | | | | | |
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| **四、引脚配置（约束文件）** | | | | | |
| NET "A[0]" LOC = T5;  NET "A[1]" LOC = V8;  NET "A[2]" LOC = U8;  NET "A[3]" LOC = N8;  NET "B[0]" LOC = M8;  NET "B[1]" LOC = V9;  NET "B[2]" LOC = T9;  NET "B[3]" LOC = T10;  NET "C0" LOC = B8;  NET "F[0]" LOC = T11;  NET "F[1]" LOC = R11;  NET "F[2]" LOC = N11;  NET "F[3]" LOC = M11;  NET "C4" LOC = V15; | | | | | |
| **五、思考与探索** | | | | | |
| 1.  2.  module module(A,B,C0,F,C8);  input [7:0] A,B;  input C0;  output [7:0] F;  output C8  wire [7:0] A;  wire [7:0] B;  wire C0;  wire [7:0] F;  wire C8;  assign F[0] = A[0]^~B[0]^~C0;  assign C1 = (A[0]&B[0])|((A[0]|B[0])&C0);  assign F[1] = A[1]^~B[1]^~C1;  assign C2 = (A[1]&B[1])|((A[1]|B[1])&C1);  assign F[2] = A[2]^~B[2]^~C2;  assign C3 = (A[2]&B[2])|((A[2]|B[2])&C2);  assign F[3] = A[3]^~B[3]^~C3;  assign C4 = (A[3]&B[3])|((A[3]|B[3])&C3);  assign F[4] = A[4]^~B[4]^~C4;  assign C5 = (A[4]&B[4])|((A[4]|B[4])&C4);  assign F[5] = A[5]^~B[5]^~C5;  assign C6 = (A[5]&B[5])|((A[5]|B[5])&C5);  assign F[6] = A[6]^~B[6]^~C6;  assign C7 = (A[6]&B[6])|((A[6]|B[6])&C6);  assign F[7] = A[7]^~B[7]^~C7;  assign C8 = (A[7]&B[7])|((A[7]|B[7])&C7);  endmodule  3.  input [15:0] A,B;  input C0;  output [15:0] F;  output C16  wire [15:0] A;  wire [5:0] B;  wire C0;  wire [5:0] F;  wire C16;  wire C4,C8,C12;  module M1(A[3:0],B[3:0],C0,F[3],C4);  module M2(A[7:4],B[7:4],C4,F[7],C8);  module M3(A[11:8],B[11:8],C8,F[11],C12);  module M4(A[15:12],B[15:12],C12,F[15],C16);  4. 不知道怎么引用模块，仿真代码不知道要加4’b，出了不少错误，通过百度解决 | | | | | |
| **六、意见和建议** | | | | | |
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